NON-VOLATILE MEMORY DEVICE WITH SELF TEST

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ABSTRACT

Self-test instructions are loaded from a tester into a configuration array of a memory device, and then a control circuit of the memory device sequentially reads and executes the self-test instructions while the tester is in an idle state. Data patterns are written to a main memory array of the memory device, the internal self-test process. The control circuit includes a comparator for detecting defective memory cells by comparing data values read from the main array with the data pattern previously written into the main memory array. A BIN counter identifies the currently-executed self-test instruction, and is read and transmitted to the tester when an error is detected.